URMIA UNIVERSITY

IRAN

DESIGN OF AN ANALOG RAM (ARAM) CHIP WITH 10-bit RESOLUTION AND LOW-POWER FOR SIGNAL PROCESSING IN 0.5 -μm CMOS PROCESS

A thesis submitted in partial satisfaction of the
requirements for the degree Master of Science
in Electrical Engineering

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2002

Happy is the gambler

who gambled away all things,

Nothing remained him

except

aspire at another gamble.

۱۳۸۱ / ۸ / ۱۵

(molana)

To:

My Parents

and

My Motherland

KURDISTAN

VITA

Kamran Hasanifard

June 21, 1974 — Born, Tehran, Iran

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ACKNOWLEDGMENTS

I would also like to thank my thesis committee members, Dr. Reiesi and Dr. Ghobadi for taking their time to serve on my committee.

I thank my parents very much for their patience among these years. I would also like to thank Dr. Komarizadeh and Dr. sadeghi so much for all their supports and Mrs. Sarhangi for her guidance. I thank my brothers and my sisters that they had so patience. And finally I would also like to thank my friends and collegians in the UMRC for the informative discussions, especially Mr. Jalili, Sharafi, Ahmadinia, Meftahi, Aghaei, Sayyahi, Ghanbari, Ahmadian, Pireh, Shayegan Mehr, Soltani, Emadi, Amin–Roaya, Peyravi, Babazadeh, Dastmalforoush, Hashemi, and especially Mrs. Katayoon Nedaei for her helps.

ABSTRACT

For analog signal processing in neural networks, we need an analog memory unit, which has flexibility and reliability to storage the analog information avoiding data conversion. This analog memory unit must has enough resolution, high speed, enough retention time, low power consumption, and small physical size.

To implementation of this system, some efforts have been done and some structures have been used. All of these structures are based on S/H architecture with switched capacitor circuits and have used an OPAMP for each line as comparator. This causes the physical size of chip be increased.

In this work, we proposed a structure with only one OPAMP as sense amplifier for whole memory lines in unit cell array. In this way, we can decrease power consumption and size of chip. By optimizing the size of transistors (Switches) and storage capacitors and trade off between speed and accuracy, we obtained writing and reading time about 35 nsec and retention time equal to 8.9 msec. The resolution of proposed ARAM is 59 dB (about 10 bits) and power consumption is 4.3 mw.

Hence, we decreased writing and reading time about 65 nsec and increased the resolution about 2 bits.

All of these circuits have been simulated with HSPICE analysis software in 0.5-μm CMOS process.

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Introduction

Cellular Neural Networks (CNN's) are analog nonlinear dynamic processor arrays in which direct interconnections among the basic processing units are restricted to a finite local neighborhood [39]. Because of their parallel processing architecture, CNN's achieve a high computation speed in the realization of their tasks. Besides, their uniformity and local connectivity make them especially suited for VLSI implementation [57]-[58].

One approach to using small-size CNN chips for large images is time-multiplexing. The time-multiplexed approach requires the definition and development of an

appropriate hardware platform for the CNN processor: the CNN chipset [60]. It is designed to support high-speed data transmission and interfacing of the analogic processor to the sensory devices and the digital host circuitry.

The Analog RAM (ARAM) is one of the non-standard parts of this chipset. It is a high-speed, short-term memory buffer that operates as the cache memory of the CNN processor. A straightforward realization of the required functionality would be the use of a conventional digital RAM interfaced with A/D and D/A converters. However, the resulting I/O rates between the memory and the processor would render this solution impractical. In order to realize a direct data interchange between the memory and the processor, avoiding data conversion, the implementation of a truly analog RAM chip is proposed. For full compatibility with the digital host environment and reduced fabrication cost, this ARAM should be designed using Standard CMOS.

In chapter 2, we explained some candidates for analog memory and advantage and disadvantage of each them has been investigated.

In chapter 3, we described some analog random access memory structures using sample and hold device.

In chapter 4, we have proposed an analog random access memory configuration with simulation results. These simulations have been done with H-SPICE software in 0.5 μm CMOS technology.

In chapter 5, we have compared between our simulation results and some structures introduced in chapter 3.

2

Theory of Analog Memory

In the CNN Universal Machine- that has been demonstrated to be universal in the Turing sense [35]- programmable nonlinear analog dynamics are combined with programmable logic operations and analog and logic distributed memories.

For the implementation of the programmable analog dynamics, the CNN core contains the integrator and the limiter blocks. Synaptic operators can be considered a part of the analog processing unit. A local logic unit (LLU) realizes programmable logic operations between stored binary magnitudes. Short-term storage of