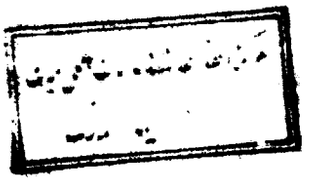
In the name of god

the compassionate,

the merciful



URMIA UNIVERSITY
IRAN

A 10-Bit 50-MS/s PARALLEL SUCCESSIVE-APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

A thesis submitted in partial satisfaction of the
requirements for the degree Master of Science
in Electrical Engineering

by
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1998

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ABSTRACT

A 10-bit 50-MS/s Parallel Successive-Approximation Analog-to-Digital Converter

by

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Applications such as high-definition video reproduction, portable computers, wireless, and multimedia demand, an ever-increasing need for high-frequency high-resolution and low-power Analog-to-Digital converters. Flash, two-step flash, and pipeline converters are fast but consume large amount of power and require large area. To overcome these problems, successive approximation converter blocks can operate in parallel to achieve high speed conversion while require low power and small area. This method relaxes considerably comparator speed. Based on this concept, a converter comprised of six successive-approximation converters operating in parallel, was designed.

The converter designed in a double-metal double-poly 1.2−μm CMOS process, achieves 50-MS/sec 10-bit conversion. This converter consumes 300-mW power with die area of about 5-mm^2. Total harmonic distortion (THD) of converter is -61dB.

1

INTRODUCTION

The proliferation of digital computing and signal processing in electronic systems is often described as "the world is becoming more digital every day". Compared with analog counterparts, digital circuits exhibit lower sensitivity to noise and more robustness to supply and process variations, allow easier design and test automation, and offer extensive programmability. But, the primary factor which has made digital circuits and processors ubiquitous in all aspects of our lives is the boost in digital performance as a result of advances in integrated circuit technologies. In particular, large scale integration (VLSI) has allowed new generations of digital circuits to attain high speed, more functionality per chip, low power dissipation, and low cost. These trends have also been augmented by circuit and architecture innovations, as well as improved analysis and synthesis computer aided design (CAD) tools.

While merits of digital circuits provide a strong incentive to make the world digital, two aspects of our physical environment impede such globalization:

a) naturally occurring signals are analog.

b) human beings perceive and retain information in analog form (at least on a macroscopic scale).

In order to interface digital processors with the analog world, analog-to-digital converters (ADCs) to acquire and digitize signals at the front end, and digital-to-analog converters (DACs) to reproduce signals at the back end, must be used. This is illustrated in Fig. 1. 1.

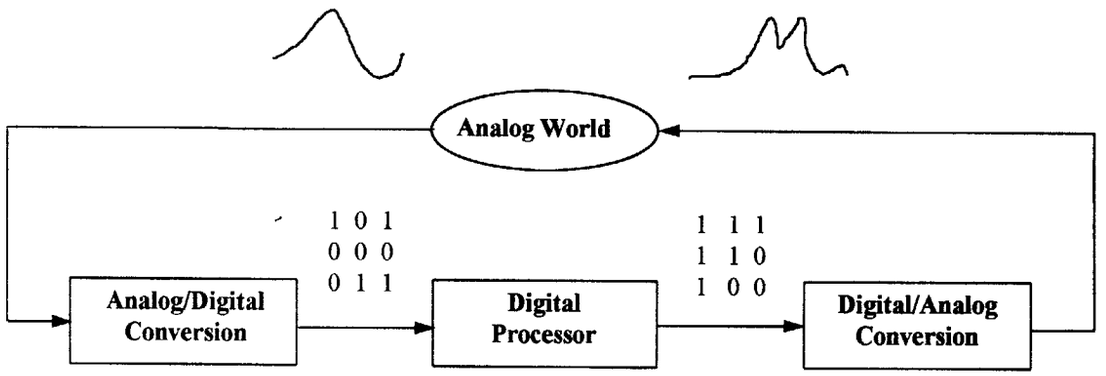

Fig. 1. 1 Interface between analog world and a digital processor.

Data converters find application in consumer products such as compact disc players, camera recorders (camcorders), telephones, modems, high-definition television (HDTV), as well as in specialized systems such as medical imaging, speech processing, instrumentation, industrial control, and radar.

Analog-to-digital converters provide the link between the analog world and digital systems. Due to extensive use of analog and mixed analog-digital operations, ADCs often appear as the bottleneck in data processing applications, limiting the overall speed or precision.

There is an ever-increasing need for monolithic analog-to-digital converters with resolutions up to 10-bit and with sample rates higher than 50-MS/s, for such applications as HDTV[1], high frequency digital communications[2], and

waveform acquisition/instrumentation. There is also a trend for the analog/digital interface to move closer to the source signal, necessitating higher ADC sample rates. Solutions with these speeds and resolution capabilities already exist in bipolar technology, for example, the folding/interpolation architecture has been shown to be an effective approach [3]. The motivation for CMOS design is that higher levels of integration and in certain occasions lower levels of power consumption than in bipolar implementations are possible. In summary, the key motivation for this work is to maximize ADC sample rate, with reasonable power and area, in CMOS.

This thesis consists of three chapters. In chapter 2, "system design", first, conventional analog-to-digital conversion architectures are introduced and are compared. Then time-interleaved architecture and its associated problems are explained. In chapter 3, "circuit design", building blocks of a successive approximation converter are presented in details. Then, problems due to mismatch among successive approximation converter are explained. Finally, HSPICE analyses results are shown.

2

SYSTEM DESIGN

Design of a 10-bit 50MS/s ADC is wanted. This converter must require low area, consume little power, and create low harmonic distortion. Thus, in this chapter, first, high speed A/D conversion architectures of flash, two-step flash, and pipeline are explained. Then, time-interleaving of successive-approximation converters are introduced. This latter architecture, is then compared to the other time-interleaved architectures. Finally a successive-approximation ADC is explained with block diagram.

2.1. High Speed A/D Converters

Flash converters, conceptually the simplest and potentially the fastest, employ parallelism and distributed sampling to achieve a high conversion rate. They need 2^m-1 compactors for an m-bit resolution, as is shown in Fig. 2. 1.

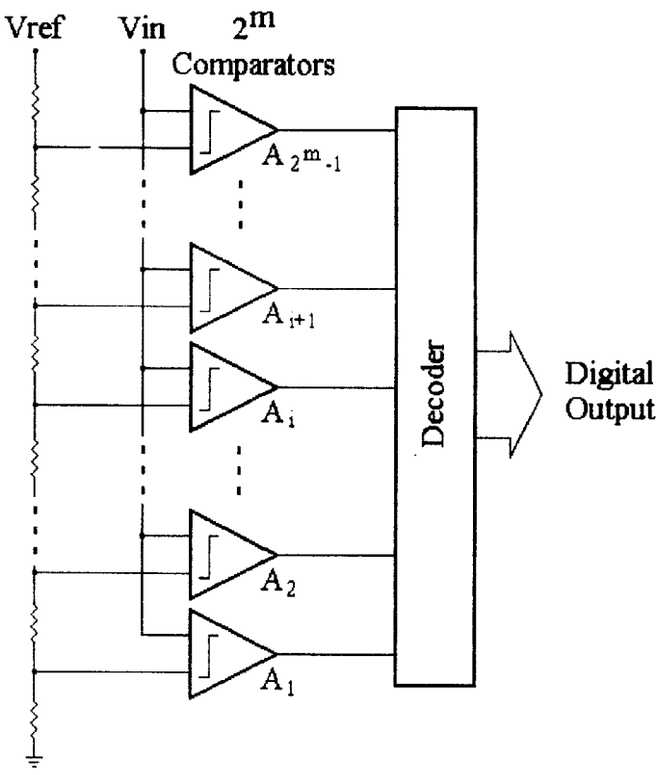

Fig. 2. 1 Block diagram of an m-bit flash A/D converter.

The exponential growth of power consumption, area, and input capacitance as a function of resolution make flash ADCs impractical for resolutions above 8 bits, calling for other topologies which can provide a more relaxed trade-off among their parameters. Two-step architectures trade speed for lower power, less area, and reduced input capacitance [4]. In a two-step flash ADC, first a coarse analog estimate of the input is obtained to yield a small voltage range around the input level. Subsequently, the input level is determined with higher precision within this range. Fig. 2. 2 shows block diagram of a two-step flash ADC. An $m=m_1+m_2$ bit two-step flash ADC consists of a front-end sample-and-hold, an m_1-bit coarse flash ADC stage, an m_1-bit DAC, a subtractor, and an m_2-bit fine flash ADC stage. Note that, DAC must have m-bit linearity.