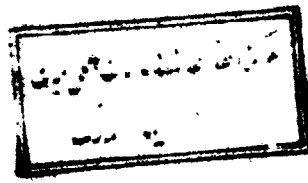


In the name of god

the compassionate,

the merciful

JFYY /11/ ۲۵



URMIA UNIVERSITY
IRAN

**A 10-Bit 50-MS/s PARALLEL
SUCCESSIVE-APPROXIMATION
ANALOG-TO-DIGITAL CONVERTER**

A thesis submitted in partial satisfaction of the
requirements for the degree Master of Science
in Electrical Engineering

by

Hamidreza Ghoddami

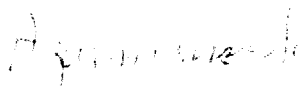
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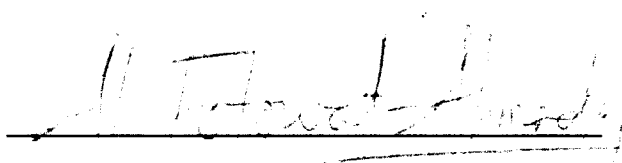
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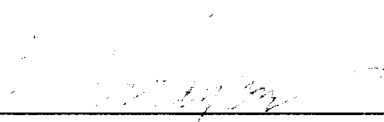
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1998

TO

MY PARENTS

List of Contents

LIST OF FIGURES AND TABLES	VI
ACKNOWLEDGMENTS	IX
ABSTRACT	X
1. INTRODUCTION	1
2. SYSTEM DESIGN	4
2.1. HIGH SPEED A/D CONVERTER	4
2.2. TIME-INTERLEAVED ARCHITECTURE	9
2.3. SUCCESSIVE-APPROXIMATION CONVERTERS	11
3. CIRCUIT DESIGN	14
3.1. DAC, S/H, AND SUBTRACTOR CIRCUITS	14
3.2. MISMATCH IN CAPACITOR RATIOS	23
3.3. COMPARATOR CIRCUIT	24
3.4. LOGIC CONTROL UNIT	37
3.5. PERFORMANCE LIMITATIONS	52
4. LAYOUT AND HSPICE ANALYSES	57
4.1. LAYOUT	57
4.2. HSPICE ANALYSES	63
4.3. CONCLUSION	68
APPENDIX	70
REFERENCES	72

List of Figures and Tables

FIG. 1. 1	INTERFACE BETWEEN ANALOG WORLD AND A DIGITAL PROCESSOR... 2
FIG. 2. 1	BLOCK DIAGRAM OF AN M-BIT FLASH A/D CONVERTER..... 5
FIG. 2. 2	BLOCK DIAGRAM OF A TWO-STEP FLASH ADC. 6
FIG. 2. 3	TWO-STEP RECYCLING ARCHITECTURE. 6
FIG. 2. 4	GENERAL PIPELINED ADC ARCHITECTURE. 7
FIG. 2. 5	BLOCK DIAGRAM OF A SUCCESSIVE APPROXIMATION A/D CONVERTER..... 8
FIG. 2. 6	A)BLOCK DIAGRAM AND B)TIMING DIAGRAM OF A TIME- INTERLEAVED ADC 10
FIG. 3. 1	AN UNIPOLAR ADC BLOCK DIAGRAM. 15
FIG. 3. 2	A 10-BIT FULLY DIFFERENTIAL A/D CONVERTER. 17
FIG. 3. 3	A NEW DAC ARCHITECTURE. 19
FIG. 3. 4	THE EQUIVALENT CIRCUIT IN SAMPLING MODE. 20
FIG. 3. 5	TRANSIENT OF INPUT SAMPLING IN WORST CASE. 21
FIG. 3. 6	THE EQUIVALENT CIRCUIT FOR DETECTION OF FIRST THREE BITS. ... 22
FIG. 3. 7	TRANSIENT OF SDS THROUGH LARGE SIZE SWITCHES S_2 TO S_9 22
FIG. 3. 8	THE EQUIVALENT CIRCUIT FOR DETECTION OF LAST SEVEN BITS. 23
FIG. 3. 9	TRANSIENT OF SDS THROUGH SMALL SIZE SWITCHES S_{10} TO S_{24} 23
FIG. 3. 10	THE COMPARATOR CIRCUIT. 25
FIG. 3. 11	A) THE INPUT OF COMPARATOR IN SAMPLING MODE, AND B) ITS SMALL-SIGNAL EQUIVALENT CIRCUIT. 26
FIG. 3. 12	THE EQUIVALENT DIFFERENCE-MODE HALF-CIRCUIT FOR CALCULATION OF A_D 27
FIG. 3. 13	TRANSIENT OF TWO STAGE OUTPUT FOR AN PULSE INPUT OF $10mV$.28

FIG. 3. 14	A)THE EQUIVALENT COMMON-MODE HALF-CIRCUIT AND B)SMALL SIGNAL EQUIVALENT CIRCUIT FOR CALCULATION OF A_c	29
FIG. 3. 15	COMMON-MODE INPUT AND OUTPUT OF FIRST STAGE.	29
FIG. 3. 16	SIMPLED CIRCUIT OF ONE STAGE FOR FREQUENCY ANALYSIS.	30
FIG. 3. 17	TRANSIENT OF TWO STAGE OUTPUT FOR AN PULSE INPUT OF $10mV$.31	
FIG. 3. 18	EQUIVALENT CIRCUIT FOR LATCH SETTLLING TIME CALCULATION..	32
FIG. 3. 19	TRANSIENT OF LATCH WITH AN INPUT OF $50mV$	32
FIG. 3. 20	COMMON-MODE HALF-CIRCUIT FOR CALCULATION OF A_{CMF}	33
FIG. 3. 21	COMMON-MODE FEEDBACK LOOP GAIN ANALYSIS RESULT.....	34
FIG. 3. 22	SIMPLIFIED CIRCUIT FOR IN OFFSET VOLTAGE CANCELLING PROCESS.....	34
FIG. 3. 23	OUTPUT BITS OF SIX CONVERTER BLOCKS.	38
FIG. 3. 24	CLOCK SIGNALS $\Phi_i, i=1, 2, \dots, 12$	39
FIG. 3. 25	LATCH AND ITS OUTPUT BUFFER.	40
FIG. 3. 26	THE USED D-FLIP-FLOPS WITH A)LOW ACTIVE RESET PIN (DFFR1) AND B) LOW ACTIVE SET PIN (DFFS1).....	41
FIG. 3. 27	OUTPUT BITS OF OVERALL ADC.....	42
FIG. 3. 28	PRODUCTION OF TIMING SIGNALS OF $\Phi_i, i=1,2,\dots,12$	45
FIG. 3. 29	PRODUCTION OF TIMING SIGNALS OF Φ_{X_i}	46
FIG. 3. 30	TIMING SIGNALS OF $\Phi_{X_{6,8,10}}$ FOR ALL OF SIX CONVERTER BLOCKS.	47
FIG. 3. 31	IMPLEMENTATION OF BOOLIAN EXPRESSIONS WITH LOGIC GATES (CONTINUED).....	49
FIG. 3. 32	LOGIC GATES USED IN LOGIC CONTROL UNIT.	51
FIG. 3. 33	CHANNEL OFFSET MISMATCH AND ITS EFFECT IN THE FREQUENCY DOMAIN.....	52
FIG. 3. 34	CHANNEL GAIN MISMATCH AND ITS EFFECT IN THE FREQUENCY DOMAIN.....	54
FIG. 3. 35	RANDOM SAMPLING JITTER.....	55

FIG. 3. 36	SYSTEMATIC TIMING MISMATCH/SKEW AND ITS EFFECT IN THE FREQUENCY DOMAIN FOR A SINUSOIDAL INPUT AT FREQUENCY F_{IN} .	56
FIG. 4. 1	OVERALL LAYOUT OF ADC CHIP	58
FIG. 4. 2	LAYOUT OF ONE SUCCESSIVE APPROXIMATION CONVERTER BLOCK.	59
FIG. 4. 3	LAYOUT OF COMPARATOR.	60
FIG. 4. 4	LAYOUT OF CAPACITOR ARRAY FOR ONE CONVERTER BLOCK.....	61
FIG. 4. 5	CAPACITOR ARRAY.....	62
FIG. 4. 6	OPERATION OF COMPARATOR IN WORST CASE WITH OFFSET CANCELLATION.....	64
FIG. 4. 7	PLOT OF THE POWER DENSITY SPECTRUM OF DIGITAL OUTPUT WITHOUT ANY MISMATCH.	65
FIG. 4. 8	PLOT OF POWER DENSITY SPECTRUM OF DIGITAL OUTPUT WITH CAPACITORS MISMATCH.....	66
FIG. 4. 9	SIMULATED THD AS A FUNCTION OF INPUT FREQUENCY.	67
FIG. 4. 10	SIMULATED THD AS A FUNCTION OF CONVERSION RATE.	67
TABLE 3. 1	HSPICE SIMULATION RESULTS OF NOISE ANALYSIS.....	35
TABLE 3. 2	STATES OF DAC SWITCHES AS A FUNCTION OF LAST BITS.....	42
TABLE 3. 3	BOOLEAN EXPRESSIONS OF DAC SWITCHES.....	48
TABLE 4. 1	SOME CHARACTERISTICS OF DESIGNED ADC.....	68
TABLE 4. 2	SOME CHARACTERISTICS OF DESIGNED ADC COMPARED TO THE RECENTLY REPORTED ADCS.....	69

ACKNOWLEDGMENTS

I would like to thank Prof. Kh. Hadidi for all the guidance he has given me all these years at urmia university.

I would like to thank my thesis committee members, professors Fotowat Ahmadi, Azarmanesh, and Abbaspour for taking the time to serve on my committee.

I thank Mr. Niknafs and Mrs. Touri in computer lab and Mrs. Sarhangi for their helps.

Finally, I would like to thank all of my friends for the informative discussions and sincerities that made my years at urmia university most enjoyable.

ABSTRACT

A 10-bit 50-MS/s Parallel Successive- Approximation Analog-to-Digital Converter

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Master of Science in Electrical Engineering

Urmia University, Iran, 1998

Applications such as high-definition video reproduction, portable computers, wireless, and multimedia demand, an ever-increasing need for high-frequency high-resolution and low-power Analog-to-Digital converters. Flash, two-step flash, and pipeline converters are fast but consume large amount of power and require large area. To overcome these problems, successive approximation converter blocks can operate in parallel to achieve high speed conversion while require low power and small area. This method relaxes considerably comparator speed. Based on this concept, a converter comprised of six successive-approximation converters operating in parallel, was designed.

The converter designed in a double-metal double-poly 1.2- μm CMOS process, achieves 50-MS/sec 10-bit conversion. This converter consumes 300-mW power with die area of about 5-mm². Total harmonic distortion (THD) of converter is -61dB.

1

INTRODUCTION

The proliferation of digital computing and signal processing in electronic systems is often described as “the world is becoming more digital every day”. Compared with analog counterparts, digital circuits exhibit lower sensitivity to noise and more robustness to supply and process variations, allow easier design and test automation, and offer extensive programmability. But, the primary factor which has made digital circuits and processors ubiquitous in all aspects of our lives is the boost in digital performance as a result of advances in integrated circuit technologies. In particular, large scale integration (VLSI) has allowed new generations of digital circuits to attain high speed, more functionality per chip, low power dissipation, and low cost. These trends have also been augmented by circuit and architecture innovations, as well as improved analysis and synthesis computer aided design (CAD) tools.

While merits of digital circuits provide a strong incentive to make the world digital, two aspects of our physical environment impede such globalization:

- a) naturally occurring signals are analog.

b) human beings perceive and retain information in analog form (at least on a macroscopic scale).

In order to interface digital processors with the analog world, analog-to-digital converters (ADCs) to acquire and digitize signals at the front end, and digital-to-analog converters (DACs) to reproduce signals at the back end, must be used. This is illustrated in Fig. 1. 1.

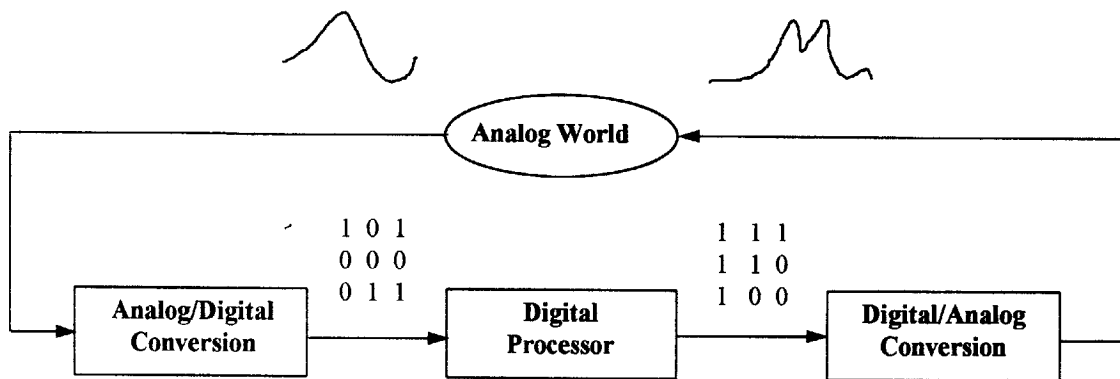


Fig. 1. 1 Interface between analog world and a digital processor.

Data converters find application in consumer products such as compact disc players, camera recorders (camcorders), telephones, modems, high-definition television (HDTV), as well as in specialized systems such as medical imaging, speech processing, instrumentation, industrial control, and radar.

Analog-to-digital converters provide the link between the analog world and digital systems. Due to extensive use of analog and mixed analog-digital operations, ADCs often appear as the bottleneck in data processing applications, limiting the overall speed or precision.

There is an ever-increasing need for monolithic analog-to-digital converters with resolutions up to 10-bit and with sample rates higher than 50-MS/s, for such applications as HDTV[1], high frequency digital communications[2], and

waveform acquisition/instrumentation. There is also a trend for the analog/digital interface to move closer to the source signal, necessitating higher ADC sample rates. Solutions with these speeds and resolution capabilities already exist in bipolar technology, for example, the folding/interpolation architecture has been shown to be an effective approach [3]. The motivation for CMOS design is that higher levels of integration and in certain occasions lower levels of power consumption than in bipolar implementations are possible. In summary, the key motivation for this work is to maximize ADC sample rate, with reasonable power and area, in CMOS.

This thesis consists of three chapters. In chapter 2, "system design", first, conventional analog-to-digital conversion architectures are introduced and are compared. Then time-interleaved architecture and its associated problems are explained. In chapter 3, "circuit design", building blocks of a successive approximation converter are presented in details. Then, problems due to mismatch among successive approximation converter are explained. Finally, HSPICE analyses results are shown.

2

SYSTEM DESIGN

Design of a 10-bit 50MS/s ADC is wanted. This converter must require low area, consume little power, and create low harmonic distortion. Thus, in this chapter, first, high speed A/D conversion architectures of flash, two-step flash, and pipeline are explained. Then, time-interleaving of successive-approximation converters are introduced. This latter architecture, is then compared to the other time-interleaved architectures. Finally a successive-approximation ADC is explained with block diagram.

2.1. High Speed A/D Converters

Flash converters, conceptually the simplest and potentially the fastest, employ parallelism and distributed sampling to achieve a high conversion rate. They need 2^m-1 comparators for an m-bit resolution, as is shown in Fig. 2. 1.

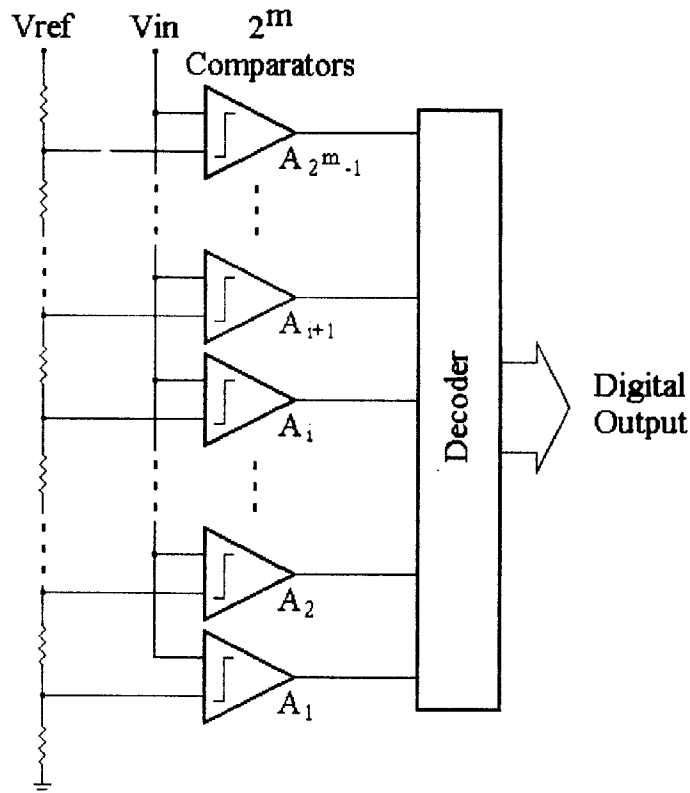


Fig. 2. 1 Block diagram of an m-bit flash A/D converter.

The exponential growth of power consumption, area, and input capacitance as a function of resolution make flash ADCs impractical for resolutions above 8 bits, calling for other topologies which can provide a more relaxed trade-off among their parameters. Two-step architectures trade speed for lower power, less area, and reduced input capacitance [4]. In a two-step flash ADC, first a coarse analog estimate of the input is obtained to yield a small voltage range around the input level. Subsequently, the input level is determined with higher precision within this range. Fig. 2. 2 shows block diagram of a two-step flash ADC. An $m=m_1+m_2$ bit two-step flash ADC consists of a front-end sample-and-hold, an m_1 -bit coarse flash ADC stage, an m_1 -bit DAC, a subtractor, and an m_2 -bit fine flash ADC stage. Note that, DAC must have m-bit linearity.