In the Name of God the compassionate the merciful

Razi University

Faculty of Engineering
Department of Electrical Engineering

Ph.D. Thesis

Title of the Thesis:

Modeling and Nonlinear Analysis of Class-E Power Amplifier with Performance Modification

Supervisor:

Dr. Mohsen Hayati

By:

Ali Lotfi

Nov 2013

Acknowledgments

This thesis would not have been possible without help and support from others. My first and sincere appreciation goes to Dr. Mohsen Hayati, my senior supervisor for all I have learned from him and for his continuous help and support in all stages of this thesis. I would also like to thank him for being an open person to ideas, and for encouraging and helping me to shape my interest and ideas. His constant encouragement, support, and invaluable suggestions made this thesis successful.

I would like to thank my committee members Professor. Abdol Ali Abdipour, Dr. Arash Ahmadi, and Dr. Gholam Reza Karimi for their interest in my work. I would like to acknowledge them for reviewing my thesis and providing valuable feedback. I am very grateful to Dr. Hiroo Sekiya of Chiba University and Professor Marian K. Kazimierczuk of Wright State University for their help and valuable advice.

I would like to acknowledge the Department of Electrical Engineering at RAZI University. I am deeply and forever indebted to my parents for their love, support and encouragement throughout my entire life. I am also very grateful to my sisters, and to my brothers.

Abstract:

Switching-Mode power amplifiers have become one of the most attractive amplification techniques due to its low dependency and sensitivity to disturbances and tolerances of the element values. This dissertation addresses the modeling and analysis of the class-E power amplifier by taking into account the linear and nonlinear characteristics of the switching device along with the duty ratio. Moreover, the performance modifications are done to obtain high-power conversation efficiency and output power capability at high-operating frequencies. A novel sub-nominal operation of the class-E power amplifier with a shunt inductor is introduced to obtain the maximum output power capability and operating frequency. The sub-nominal condition means that only the zero-current switching condition (ZCS) is achieved, though the nominal conditions mean that both the ZCS and zero-current derivative switching (ZCDS) are satisfied. The design values for achieving the sub-nominal condition are expressed as a function of the phase shift between the input and output voltages. The class-E amplifier with sub-nominal condition increases one design degree of freedom compared with that with the nominal conditions. Because of the increase in the design degree of freedom, one more relationship can be specified as a design specification. Therefore, it is possible to specify an additional condition such as output power, power conversion efficiency, total harmonic distortion (THD), peak switch voltage, and peak switch current instead of the ZCDS condition. In the sub-nominal operation with any duty ratio, both the peak switch voltage and the peak switch current can be set as design specifications due to two more degrees of design freedom in comparison with the class-E nominal amplifier at the fixed duty ratio. Additionally, it is also seen that the duty ratio affects the maximum operating frequency and the output power capability with ZCS condition.

In the class-E power amplifier with a shunt capacitance, the linear and nonlinear parasitic capacitance of the switching device is considered for modeling of the class-E power amplifier to satisfy the class-E ZVS and ZVDS conditions. In this case, the duty ratio is used not only as the design specification, but also as the adjustment parameter for achieving a certain condition. The optimization of the drain efficiency for lower supply voltages can be achieved by the reduction of the peak switch voltage. It is done by taking into account the duty ratio as a design specification and properly choosing the value of dc-supply voltage. The maximum operating frequency, output power capability, and element values as functions of the duty ratio are obtained. The element values are directly

dependent upon the selection of duty ratio and require a careful duty ratio selection to minimize component power losses and to maximize the total efficiency.

The external shunt capacitance is used in the parallel form with the switching device to consider the output power as design specification for the class-E shunt capacitance power amplifier with the MOSFET linear and nonlinear parasitic capacitances. The class-E power amplifier characteristics are obtained as functions of the ratio of the sum of the external shunt capacitance and the MOSFET gate-to-drain capacitance to the MOSFET drain-to-source junction capacitance at v_s=0. The design procedure by taking into account the load-resistance or output power as design specification is described. Although, the effect of the MOSFET linear gate-to-drain capacitance is similar to that of the external linear shunt capacitance on the design of the class-E power amplifier with the square-input voltage, the difference between their effects should be considered for the sinusoidal-input voltage. Additionally, analytical expressions of output power capability and power conversion efficiency are given, which are considerable affected by the external linear shunt capacitance.

The analytical expressions for waveforms and design relationships are derived for the class-E power amplifier with the MOSFET nonlinear drain-to-source parasitic capacitance at the sub-nominal operation, i.e., only zero voltage switching (ZVS) condition, for any grading coefficient *m* of the MOSFET body junction diode and 50% duty ratio. Only the MOSFET nonlinear drain-to-source parasitic capacitance is used in the analysis of the class-E ZVS power amplifier, which its nonlinearity is determined by the grading coefficient *m*. The grading coefficient *m* is used as an adjustment parameter to satisfy the given output power and peak switch voltage simultaneously. Additionally, the output power capability and maximum operating frequency are affected by the grading coefficient *m*. The validity of the analytical expressions in this dissertation is verified with a simulation by circuit simulator and measurement results for all proposed power amplifiers. The measurement and simulation results agreed with the analytical expressions quantitatively, which show the validity of our analytical expressions.

Contributions of this dissertation have been published in four JCR-indexed journal papers (IEEE-Transactions).

Table of Contents

Page

Chapter 1: Introduction 1
- 1-1- Motivation and Objectives……. 2
- 1-2- Background and Review of Previous Research……... 3
- 1-3- Operating Classes of Power Amplifiers……. 6
- 1-4- Class-E Operation Family…….. 14
- 1-5- Class-F Operation Mode……. 20
- 1-6- Thesis Outline……. 25

Chapter 2: Class-E Power Amplifier Family 27
- 2-1- Introduction…….. 28
- 2-2- Class-E Configurations and Conditions…….. 29
  - 2-2-1- Class-E with a Shunt Capacitance Topology…….. 30
  - 2-2-2- Class-E with a Shunt Inductor Topology…… 36
- 2-3- Class-E Power Amplifier Analysis Methodologies…… 39
  - 2-3-1- Assumptions and Circuit Descriptions…….. 41
  - 2-3-2- Analytical Methods…….. 43
  - 2-3-3- Numerical Methods…….. 44
- 2-4- Other Class-E Power Amplifier Family…….. 45
  - 2-4-1- Analysis of Class-DE Amplifier Methodology…… 46
  - 2-4-2- Analysis of Class-E_M amplifier Methodology……..... 47
- 2-5- Conclusions…… 49

Chapter 3: Class-E Power Amplifier With a Shunt Inductor For The Sub-Nominal Operation 50
- 3-1- Introduction…… 51
- 3-2- Class-E Shunt Inductor Power Amplifier Conditions…… 51
- 3-3- Sub-nominal Operation…….. 54
  - 3-3-1- Circuit Descriptions……. 54
  - 3-3-2- Switch Current and Voltage Waveforms…… 57
  - 3-3-3- Design Equations……. 65
- 3-4- Perturbation Analysis……. 67
  - 3-4-1- Output Power Capability……. 67
  - 3-4-2- Power Conversation Efficiency …….. 71
- 3-5- Simulation and the Circuit Implementation Results and Discussions…… 73
  - 3-5-1- Design Specifications…….. 73
  - 3-5-2- Design Procedure…….. 73
  - 3-5-3- Experimental Results……... 78
- 3-6- Conclusions…… 83

Chapter 4: Performance Study Of The Class-E Power Amplifier With A Shunt Inductor For The Sub-Nominal Operation At Any Duty Ratio 84
- 4-1- Introduction…… 85
- 4-2- The Class-E ZCS condition with Duty Ratio…… 85
  - 4-2-1- Circuit Descriptions…… 87
  - 4-2-2- Circuit Design for Sub-Nominal Condition at Any Duty

Ratio…… 91
4-3- Fourier Analysis…… 104
4-4- Power Conversion Analysis…… 106
4-4-1- Output Power Capability…… 106
4-4-2- Power Losses with Duty ratio…… 110
4-5- Circuit Implementation Results and Discussions…… 114
4-5-1- Design Specifications…… 114
4-5-2- Effect of the Duty Ratio on Design Procedure…… 114
4-5-3- Experimental Results with Duty ratio…… 116
4-6- Conclusions…… 119

Chapter 5: Class-E Power Amplifier With MOSFET Parasitic Capacitances 120
5-1- Introduction…… 121
5-2- Class-E ZVS and ZVDS conditions…… 121
5-3- Modeling of the Power MOSFET…… 123
5-3-1-Switching Pattern…… 123
5-3-2- Intrinsic Capacitance…… 124
5-3-3-Drive Input Voltage…… 125
5-4- Effect of the Duty Ratio…… 127
5-4-1- Circuit Waveforms Equations…… 127
5-4-2- Power Relations…… 130
5-4-3- Element Values…… 134
5-5- Switching Stresses…… 137
5-5-1- Peak Switch Voltage…… 137
5-5-2- Peak switch Current…… 138
5-5-3- Output Power Capability…… 139
5-6- Maximum Operating Frequency…… 140
5-7- Power Conversion Efficiency…… 142
5-7-1- Equivalent Series Resistance …… 142
5-7-2- Power Dissipations…… 142
5-8- Simulated and Measured Results…… 144
5-8-1- Design Procedure for Fixed and Varied Duty Ratio…… 145
5-8-2- Comparing of Results…… 146
5-9- Conclusions…… 151

Chapter 6: Class-E Power Amplifier With MOSFET Parasitic Capacitances And An External Shunt Capacitance 152
6-1- Introduction…… 153
6-2- Class-E with a Shunt Capacitance…… 154
6-2-1- MOSFET Non-Linear Intrinsic Capacitance…… 156
6-2-2- Parasitic and External Shunt Capacitances…… 157
6-3- Circuit Analysis with Linear and Nonlinear Capacitances…… 160
6-3-1- Switch Voltage and Current…… 160
6-3-2- Discussions and Comparisons for MOSFETs…… 165
6-3-3-Voltage across Resonant-Circuit Reactance and Design Equations…… 170
6-4- Switch Characteristics…… 172
6-4-1- Peak Switch Voltage and Current…… 172
6-4-2- Output Power Capability…… 175

6-4-3- Maximum Operating Frequency……. 176
6-5- Power Dissipations Analysis……. 177
6-6- Circuit Implementation……. 180
6-6-1- Design Specifications……. 180
6-6-2- Design Procedure for the Specified Output Power……. 180
6-6-3- Output Power Gain and THD……. 184
6-6-4- Results and Discussions……. 185
6-7- Conclusions……. 190

Chapter 7: Class-E ZVS Power Amplifier With MOSFET Nonlinear Capacitance For Any Grading Coefficient *m* 191
7-1- Introduction……..... 192
7-2- Class-E Sub-nominal Operation……..……. 192
7-2-1- Nominal and Optimal Operation……. 193
7-2-2- Sub-nominal Condition ……. 193
7-3- Circuit Analysis with Nonlinear Shunt Capacitance……. 196
7-3-1- Circuit Description and MOSFET Modeling…….. 196
7-3-2- Basic Waveforms at Sub-Nominal Operation……. 198
7-3-3- Design Equations……. 204
7-4- Effect of Grading Coefficient on Switch Characteristics…….. 206
7-4-1- Peak Switch Voltage and Current……... 206
7-4-2- Output Power Capability……..…… 209
7-4-3- Perturbation Analysis……..…. 210
7-5- Circuit Implementation……..……. 212
7-5-1- Design Procedure with Grading Coefficient …….. 212
7-5-2- Switching Element Selection……... 213
7-5-3- Experimental results and discussions…….. 216
7-6- Conclusions…… 222

Chapter 8: Conclusions and Future Works 223
8-1- Conclusions……..……... 224
8-2- Future Works……..…… 226
8-3- Publications……....…… 227
References…….. 229

List of Figures

Contents **Page**

Figure 1-1- The Basic circuit topology of power amplifier……..…….. 5
Figure 1-2- General circuit diagram of class-A, class-AB, class-B and class-C power amplifiers……...…..…… 7
Figure 1-3- (a) The class-A drain voltage (dash-line) and current (solid-line) waveforms. (b) The load-line……..….. 7
Figure 1-4- (a) The class-AB drain voltage (dash-line) and current (solid-line) waveforms. (b) The load-line……..... 9
Figure 1-5- (a) The class-B drain voltage (dash-line) and current (solid-line) waveforms. (b) The load-line …….…….. 10
Figure 1-6- (a) The class-C drain voltage (dash-line) and current (solid-line) waveforms. (b) The load line ……..….. 10
Figure 1-7- The class-D power amplifier (voltage-mode). (a) Idealized circuit topology. (b) Switch drain voltage and current waveforms…….…. 12
Figure 1-8- The class-D^{-1} power amplifier (current-mode). (a) Idealized circuit topology. (b) Switch drain voltage and current waveforms…….…. 13
Figure 1-9- The Class-E power amplifier with a shunt capacitance. (a) Basic circuit topology. (b) Switch voltage and current waveforms for the ideal operation……..... 15
Figure 1-10- The Class-E power amplifier with a shunt inductor. (a) Basic circuit topology. (b) Switch voltage and current waveforms for the ideal operation……..….. 16
Figure 1-11- Circuit topology of class-DE power amplifier…… 17
Figure 1-12- Nominal waveforms for class-DE power amplifier at the duty ratio 0.25……... 17
Figure 1-13- The class-E_M power amplifier circuit pology……. 18
Figure 1-14- Nominal waveforms of the class-E_M power amplifier for the duty ratio 0.5…….……. 19
Figure 1-15- (a) Class-F power amplifier circuit topology. (b) Inverse class-F power amplifier circuit topology……... 21
Figure 1-16- Nominal switch voltage and current waveforms. (a) Class-F power amplifier. (b) Inverse class-F power amplifier…….. 21
Figure 1-17- Circuit topology of class-E/F_{odd} power amplifier…… 23
Figure 1-18- Switch-voltage and current waveforms of an ideal class-E/F_{odd} power amplifier……..……. 23
Figure 2-1- The class-E power amplifier. (a) Basic circuit topology. (b) Idealized equivalent circuit……..……... 30
Figure 2-2- The basic class-E shunt capacitance power amplifier waveforms. (a) Switch voltage. (b) Output voltage. (c) Switch current. (d) Output current……. 32
Figure 2-3- The basic circuit of the class-E shunt inductor power amplifier……... 37

Figure 2-4- Steady-state waveforms for the nominal operation. (a) Shunt inductor voltage. (b) Switch voltage. (c) Switch current. (d) Output current..... 38
Figure 3-1- (a) Basic circuit of the class-E shunt inductor power amplifier [12]. (b) Idealized equivalent circuit used in this analysis [12]……...…. 54
Figure 3-2- Normalized slope of switch current as a function of φ ……. 59
Figure 3-3- $V_{DD}/I_{DD}R$ as a function of φ ……...…. 60
Figure 3-4- V_m/V_{DD} as a function of φ ……. 61
Figure 3-5- $R/\omega L$ as a function of φ …….. 62
Figure 3-6- Typical normalized switch voltage waveforms, for $\varphi > \varphi_{\text{nominal}}$, $\varphi = \varphi_{\text{nominal}}$ and $\varphi < \varphi_{\text{nominal}}$, Nominal condition, i.e., ZDCS is obtained at $\varphi = \varphi_{\text{nominal}}$.For $\varphi > \varphi_{\text{nominal}}$ and $\varphi < \varphi_{\text{nominal}}$, the switch voltage begins from the positive and negative values, respectively…….. 62
Figure 3-7- Typical Normalized switch current waveforms, for $\varphi > \varphi_{\text{nominal}}$, $\varphi = \varphi_{\text{nominal}}$ and $\varphi < \varphi_{\text{nominal}}$, Nominal condition, i.e., ZDCS is obtained at $\varphi = \varphi_{\text{nominal}}$. For $\varphi > \varphi_{\text{nominal}}$, the switch current rises up to zero. For $\varphi < \varphi_{\text{nominal}}$, the switch current falls down to zero when the switch turns off φ …….. 63
Figure 3-8- The peak of normalized shunt inductor current $i_{L,peak}R/V_{DD}$ as a function of φ …….. 65
Figure 3-9- $1/\omega C_X R$ as a function of φ …….. 67
Figure 3-10-. Normalized peak switch current $I_{SM}R/V_{DD}$ as a function of φ …… 68
Figure 3-11- Normalized peak switch voltage as a function of φ ……... 69
Figure 3-12- Output power capability c_p as a function of φ …… 70
Figure 3-13- The equivalent circuit of the class-E shunt inductor power amplifier including ESRs…… 72
Figure 3-14- Waveforms obtained from the theoretical expressions, PSpice Simulation, and experiments for the sub-nominal operation……..... 81
Figure 3-15- Comparison of the simulated and measured values of output power as a function of the load resistance for the sub-nominal condition circuit design example……. 82
Figure 3-16- Comparison of the simulated and measured values of efficiency as a function of the load resistance for the sub-nominal condition circuit design example…… 82
Figure 4-1- The class-E power amplifier with a shunt inductor. (a) Circuit topology [12]. (b) Idealized equivalent circuit [12]…… 87
Figure 4-2- φ as a function of the normalized derivative of the switch current α for fixed values of the duty ratio D……..…… 93
Figure 4-3- Normalized peak switch voltage V_{SM}/V_{DD}. (a) as a function of α for fixed values of the duty ratio D. (b) as a function of the duty ratio D for fixed values of α ……..…… 96
Figure 4-4- Typical Normalized switch voltage for $\alpha > 0$, $\alpha = 0$ and $\alpha < 0$, the

normalized peak switch voltage increases as α decreases..……...…… 97
Figure 4-5- I_m/I_{DD} . (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α …… 98
Figure 4-6- $V_{DD}/I_{DD}R$. (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α …… 98
Figure 4-7- V_m/V_{DD} . (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α ……. 99
Figure 4-8- P_oR/V_{DD}^2 (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α ……. 100
Figure 4-9- $R/\omega L$ (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α ……..…. 101
Figure 4-10- The peak of normalized shunt inductor current $i_{L,peak}/I_{DD}$. (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α ……. 102
Figure 4-11- $\omega C_x R$. (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α …….. 106
Figure 4-12- Normalized peak switch current I_{SM}/I_{DD} . (a) as a function of α for fixed values of the duty ratio *D*. (b) as function of the duty ratio *D* for fixed values of α …… 108
Figure 4-13- The output power capability c_p . (a) as a function of α for fixed values of the duty ratio *D*. (b) as a function of the duty ratio *D* for fixed values of α ……..…… 110
Figure 4-14- The equivalent circuit of the class-E shunt inductor power amplifier including ESRs…….. 113
Figure 4-15- $I_{SM}R/V_{DD}$ as a function of V_{SM}/V_{DD} for fixed values of the duty ratio *D*. …… 115
Figure 4-16- Waveforms for the circuit design example obtained from: (a) Theoretical expressions, and simulations by circuit simulator, (b) Experiments. ……..…….. 119
Figure 5-1- (a) Basic circuit of the class-E power amplifier. (b) Idealized equivalent circuit used in this analysis……..…….. 125
Figure 5-2- Class-E power amplifier waveforms for any *D*. (a) Gate-to-source driving voltage waveform. (b) Drain-to-source voltage waveform. (c) Output voltage..……. 126
Figure 5-3- φ as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540, φ decreases as D increases… 132
Figure 5-4- $\omega C_{jo}R$ as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540……..... 133
Figure 5-5- V_m/V_{DD} as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of

V_g/V_{bi} , for two MOSFETs IRF510 and IRF540..... 133
Figure 5-6- $V_{DD}/I_{DD}R$ as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540..... 134
Figure 5-7- $\omega^2 L_x C_{j0}$ as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540..... 136
Figure 5-8- $V_{s,\max}/V_{DD}$ as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540. 138
Figure 5-9- $I_{MOS,\max}/I_{DD}$ as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540..... 139
Figure 5-10- The output power capability c_p as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540. 140
Figure 5-11- The maximum operating frequency normalized by the maximum operating frequency at duty ratio 0.5, as a function of D for V_{DD}/V_{bi} =18.75, and fixed values of V_g/V_{bi} , for two MOSFETs IRF510 and IRF540. 141
Figure 5-12- Idealized equivalent circuit of the class-E power amplifier with ESRs..... 142
Figure 5-13- Class-E power amplifier waveforms at D=0.3. (a) Theoretical expressions (solid line), and PSpice simulations (dash line). (b) Circuit experiment. 149
Figure 5-14- Class-E power amplifier waveforms at D=0.7. (a) Theoretical expressions (solid line), PSpice simulations (dash line). (b) Circuit experiment..... 149
Figure 6-1- The class-E power amplifier. (a) Basic circuit topology. (b) Idealized equivalent circuit..... 158
Figure 6-2- Nominal waveforms of the class-E power amplifier. (a) Gate-to-source driving voltage waveform. (b) Drain-to-source voltage waveform. (c) Output voltage..... 159
Figure 6-3- φ as a function of V_{DD}/V_{bi} for fixed values of γ_2 , $\gamma_1 = 0$, and $V_g = 0$. (a) The IRF510 MOSFET. (b) The IRF540 MOSFET..... 166
Fig.ure 6-4- φ as a function of γ_2 for $V_{DD}/V_{bi} = 25$, and fixed values of γ_1 and V_g/V_{DD} 167
Figure 6-5- $\omega C_{j0}R$ as a function of V_{DD}/V_{bi} for fixed values of γ_2 , sinusoidal (solid line) and square (dash line) gate-source voltage. (a) The IRF510 MOSFET. (b) The IRF540 MOSFET..... 168
Figure 6-6- γ_2 as a function of $\omega C_{j0}R$ for $V_{DD}/V_{bi} = 25$, and fixed values of γ_1 and V_g/V_{DD} 169
Figure 6-7- V_m/V_{DD} as a function of γ_2 for $V_{DD}/V_{bi} = 25$, and fixed values of γ_1 and

V_g/V_{DD} 170
Figure 6-8- $V_{DD}/I_{DD}R$ as a function of γ_2 for $V_{DD}/V_{bi}=25$, and fixed values of γ_1 and V_g/V_{DD} 170
Figure 6-9- $\omega^2 C_{j0}L_x$ as a function of γ_2 for $V_{DD}/V_{bi}=25$, and fixed values of γ_1 and V_g/V_{DD} 172
Figure 6-10- $V_{S,\max}/V_{DD}$ as a function of γ_2 for $V_{DD}/V_{bi}=25$, and fixed values of γ_1 and V_g/V_{DD} 173
Figure 6-11- $I_{MOS,\max}/I_{DD}$ as a function of γ_2 for $V_{DD}/V_{bi}=25$, and fixed values of γ_1 and V_g/V_{DD} 174
Figure 6-12- c_p as a function of γ_2 for $V_{DD}/V_{bi}=25$, and fixed values of γ_1 and V_g/V_{DD} 176
Figure 6-13- $Rf_{\max}$ as a function V_{DD}/V_{bi}, for IRF510 and IRF540 MOSFETs, sinusoidal (solid-line) and square (dash-line) gate-source voltage waveform..... 177
Figure 6-14- Idealized equivalent circuit of the class-E power amplifier with ESRs. 178
Figure 6-15- Class-E power amplifier waveforms from theoretical expressions, PSpice simulations, and circuit experiment for the sinusoidal gate-to-source voltage..... 187
Figure 6-16- Class-E power amplifier waveforms from theoretical expressions, PSpice simulations, and circuit experiment for the square gate-to-source voltage. 187
Figure 7-1- The class-E ZVS power amplifier waveforms from PSpice-simulation using the elements values [81] for IRF510 MOSFET. (a) For non-zero the MOSFET nonlinear drain-to-source capacitance. (b) For zero the MOSFET nonlinear drain-to-source capacitance..... 196
Figure 7-2- Class-E power amplifier with a nonlinear shunt capacitance. (a) Basic circuit topology. (b) Idealized equivalent circuit..... 198
Figure 7-3- φ as a function of β/V_{DD} for fixed values of the grading coefficient m. 202
Figure 7-4- $\omega C_{j0}R$ as a function of β/V_{DD} for fixed values of the grading coefficient m..... 202
Figure 7-5- $V_{DD}/I_{DD}R$ as a function of β/V_{DD} for fixed values of the grading coefficient m..... 203
Figure 7-6- V_m/V_{DD} as a function of β/V_{DD} for fixed values of the grading coefficient m..... 204
Figure 7-7- $\omega L_x/R$ as a function of β/V_{DD} for fixed values of the grading coefficient m..... 206

Figure 7-8- Normalized peak switch voltage V_{SM}/V_{DD} as a function of β/V_{DD} for fixed values of the grading coefficient m. ……..……... 207
Figure 7-9- $I_{SM}R/V_{DD}$ as a function of β/V_{DD} for fixed values of the grading coefficient m…….……. 208
Figure 7-10- c_p as a function of β/V_{DD} for fixed values of the grading coefficient m…….……. 210
Figure 7-11- The equivalent circuit of the class-E power amplifier with taking into accounts ESRs of the switching device and passive elements…. 211
Figure 7-12- V_{SM}/V_{DD} as a function of P_oR/V_{DD}^2 for fixed values of the grading coefficient m…….…….…….. 213
Figure 7-13- The input, switching and output waveforms for the first design example. (a) Theoretical expressions (dash line), PSpice simulations (solid line). (b) Circuit experiment……..……..…….. 217
Figure 7-14- The input, switching and output waveforms for the second design example. (a) Theoretical expressions (dash line), PSpice simulations (solid line). (b) Circuit experiment…….……..... 219

List of Tables

Contents **Page**

TABLE 3-1- The IRF510 MOSFET characteristics…… 73
TABLE 3-2- The values of the elements for the nominal conditions and sub-nominal condition design examples…… 77
TABLE 3-3- The values of the elements and power relation for the sub-nominal design example……..…….. 80
TABLE 4-1- Switching pattern…… 88

TABLE 4-2- Theoretical predictions, simulations by circuit simulator, and experimental measurements for the circuit design example……..…. 118
TABLE 5-1- Parameters of the MOSFETs…….. 132
TABLE 5-2- The values of the elements for two circuit design examples…….. 146
TABLE 5-3- The theoretical, simulated and measured results for the first circuit design example…… 148
TABLE 5-4- The theoretical, simulated and measured results for the second circuit design example……. 150
TABLE 6-1- Switching pattern…… 160
TABLE 6-2- Parameters of the MOSFETs 165
TABLE 6-3- The IRF510 MOSFET characteristics…… 180
TABLE 6-4- The values of the elements for the sinusoidal and square gate-to-source voltage…… 183
TABLE 6-5- The theoretical, simulated and measured results for the first circuit design example…… 188
TABLE 6-6- The theoretical, simulated and measured results for the second circuit design example……. 189
TABLE 7-1- Parameters of the MOSFETs…….. 201
TABLE 7-2- The values of the elements for two circuit design examples…….. 216
TABLE 7-3- Theoretical predictions, Pspice simulations, and experimental measurements for the first circuit design example……..… 218
TABLE 7-4- Theoretical predictions, Pspice simulations, and experimental measurements for the second circuit design example……. 220

List of Abbreviations and Acronyms

AC	Alternating Current
AM	Amplitude Modulation
CAD	Computer Aided Design
CMCD	Current-Mode Class-D
CMOS	Complementary Metal Oxide Semiconductor
dB	Decibel
DC	Direct Current
DE	Disruptive Effect
ESR	Equivalent Series Resistance
FET	Field Effect Transistor
FM	Frequency Modulation
HB	Harmonic Balance
HBT	Hetero-Junction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HF	High Frequency
HFET	Hetero-Structure FET
IC	Integrated Circuit
JFET	Junction FET
MSFET	Metal Semiconductor Fet
MMIC	Monolithic Microwave Integrated Circuit
MN	Matching Network
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PHEMT	Pseudomorphic HEMT
Q	Quality Factor
RF	Radio Frequency
RFC	Radio Frequency Chock
VMCD	Voltage-Mode Class-D
ZCS	Zero Current Switching
ZCDS	Zero Current Derivative Switching
ZVS	Zero Voltage Switching
ZVDS	Zero Voltage Derivative Switching
ZCS	Zero Current Switching
ZCDS	Zero Current Derivative Switching

Nomenclature

Symbol	Description
A	Amplitude of a Signal
A_m	Magnitude of a Sine Wave Signal
c_p	Out-Put Power Capability
Cs	Shunt Capacitance
C_{ds}	Drain-to-Source Capacitance
C_{gd}	Gate-to-Drain Capacitance
C_{j0}	Zero Bias Capacitance
D	Duty Ratio
f	Operating Frequency
f_{max}	Maximum Operating Frequency
G	Power Gain
io	Output Current
is	Switch Current
I_{DD}	DC-Current
$I_{MOS,max}$	Peak Switch Current
I_R	Magnitude Of The Load Current
$LRFC$	DC-Feed
Ls	Shunt Inductance
m	Junction Grading Coefficient
P	Power
P_{DC}	Dc Power
P_{in}	Input Power
Q	Quality Factor
R	Load Resistance
V_{bi}	Built-In Potential
V_{DD}	DC-Supply Voltage
vs	Switch Voltage
vo	Output Voltage
V_T	MOS Threshold Voltage
W	MOS Channel Width

X	Reactance
X_{dc}	Reactance of the DC-Feed Inductance
Y	Admittance
Z	Impedance
Z_n	Impedance at n-th Harmonic
Z_L	Load Impedance
η	Output (Collector/Drain) Efficiency
η_{max}	Maximal Efficiency
η_{tot}	Total Efficiency
θ	Angular Time
φ	Phase
ω	Angular Frequency

Chapter One

Introduction

1-1-Motivation and Objectives:

The field of switch-mode power amplifiers has been one of the most active areas in research and development of power electronics in the last decades. One of the most important switch-mode power amplifiers is the class-E power amplifier, which is an efficient and important solution to achieve high-efficiency and high operating frequency performances in a lot of various applications, such as the radio-transmitter, dc–dc power converters, oscillator, electronic fluorescent lamp ballast, frequency multiplier, induction heating, and an RF power transmitter of the implanted system. Therefore, the research and development of the class-E power amplifier families has been a very interesting area in recent years.

One of the most extended operation types of the class-E power amplifiers with a shunt inductance is the sub-nominal operation, i.e., only zero-current switching (ZCS) condition that the degree of the design freedom is increased by one. Nevertheless, there are certain aspects with regard to these operation conditions that have not been studied in the technical literature on the matter that should be investigated in order to take the advantages of their actual potential. This research provides an in-depth analysis of uncovered issues regarding the sub-nominal and duty ratio for the class-E power amplifier with a shunt inductor.

Most of the researches devoted to the class-E power amplifier with a shunt capacitance that has been carried out in the nominal operation, which is introduced as zero-voltage switching (ZVS) and zero-voltage derivative switching (ZVDS) conditions. However, their observations and achievements cannot be applied to the design of the class-E power amplifier with arbitrary design specifications such as peak switch voltage, peak